

EE/C SC 1510 Logic Design

University of Colorado at Denver and Health Sciences Center
College of Engineering and Applied Science

Term: Fall 2009

Course days/times: Tues./Thurs. 5:30pm-6:45pm

Course location: NC1326

Office Hours: After class, 6:45pm-7:45pm,
(otherwise by appointment)

Lecturer: Anthony Jackson

Office location: NC2615, (conf. room)

Phone: 303-706-4403

email address: TBD

Web site and/or BlackBoard site: TBD

Course Information

Catalog Description: E E 1510. Logic Design. The design of combinatorial and sequential switching circuits. Topics include Boolean algebra, Boolean function minimization technique, combinatorial circuit analysis and synthesis, synchronous sequential circuit analysis and synthesis, algorithmic state machine design, asynchronous sequential circuit analysis and synthesis. Cross-listed with C SC 1510. Prereq: MATH 1120 or equivalent.

Requirements

Required Texts: "Fundamentals of Logic Design, 6th Edition" by Charles H. Roth, Jr.

Recommended Texts: "Digital Design: Principles and Practices Package (4th Edition)" by John F. Wakerly (optional, recommended for additional study beyond this course)

Additional Materials, Equipment: Xilinx ISE Webpack 11 (optional, for additional study beyond this course), Windows or Linux PC, CPLD and/or FPGA experimentation board (optional, for additional study beyond this course).

Assessment

Grading Scale:

A	90% - 100%
B	80% - 89%
C	70% - 79%
D	60% - 69%
F	< 50%

Homework	30%
Exam 1	30%
Exam 2	30%
Final	10%

Course Policies:

Homework assignments will generally be due one week after assigned (usually on a Tuesday). Homework will lose one letter grade (10%) for every class period late. Homework will typically be

returned, in class, one week after due.

Attendance is required and is in your best interest because I reserve the right to give tips on tests, assign extra credit, and otherwise make it worth your while. If you know you will miss class, try to make arrangements with another student to get notes and announcements, otherwise take advantage of office hours. If you *must* miss a test, please contact me beforehand, if possible. Cheating and plagiarism will not be tolerated and will result in a failing grade.

Course Schedule

Date	Topic	Required Reading
Aug. 18, 20	Course Introduction, Number Systems	--
Aug. 25, 27	Number Systems, Boolean Algebra	Ch 1, 2
Sept. 1, 3	Boolean Algebra	Ch 3, 4
Sept. 8, 10	Karnaugh Maps	Ch 5
Sept. 15	Karnaugh Maps, Exam 1 Review	Ch 1-5
Sept. 17	Exam 1	Ch 1-5
Sept. 22, 24	NAND, NOR gates, Combinational Circuit Design	Ch 7, 8
Sept. 29, 1	Muxes, Decoders, PLDs	Ch 9
Oct. 6, 8	Latches, Flip Flops	Ch 11
Oct. 13, 15	Registers and Counters	Ch 12
Oct. 20	Exam 2 Review	Ch 7-12
Oct. 22	Exam 2	Ch 7-12
Oct. 27, 29	Analysis of Clocked Sequential Circuits	Ch 13
Nov. 3, 5	State Graphs	Ch 14
Nov. 10, 12	Reduction of State Assignment	Ch 15
Nov. 17, 19	Sequential Circuit Design	Ch 16
Nov. 23-27	Fall Break, No Class, Study for Final	Ch 1-16 (except 6 and 10)
Dec. 1, 3	Review for Finals	Ch 1-16 (except 6 and 10)
Dec. 7-12	Finals Week	Ch 1-16 (except 6 and 10)

Course Communication

Email and Blackboard will be utilized to distribute announcements, assignments, notes, slides, etc.

Students called for military duty

- If you are a student in the military with the potential of being called to military service and /or training during the course of the semester, you are encouraged to contact Paul Rakowski.