

**EE 1510-001 Logic Design
Fall 2009**

University of Colorado at Denver
College of Engineering and Applied Science

Course dates/times: MW 4:00-5:15 pm

Course location: WC 140

Instructor: Kelly Campbell

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Office: NC 2404C

Office Hours: M 3:00 – 4:00 pm, W Noon – 1:00 pm

Course Catalogue Description:

The design of combinatorial and sequential switching circuits. Topics include Boolean algebra, Boolean functions, minimization techniques, combinatorial circuit analysis and synthesis, synchronous sequential circuit analysis and synthesis, algorithmic state machine design, asynchronous sequential circuit analysis and synthesis.

Prerequisite: Math 1120 College Trigonometry or equivalent

Required Text: Fundamentals of Logic Design, Charles H. Roth, Jr., 6th Edition. ISBN 0-495-66804-4

Assessment:

Exam 1 (Sep. 16)	20%
Exam 2 (Oct. 14)	20%
Exam 3 (Nov. 11)	20%
Final Exam (date to be determined)	30%
Homework and quizzes	10%

- The final exam will be comprehensive and administered during finals week.
- Make-up of exams will only be permitted if prior arrangements are made, at the discretion of the instructor, or in the case of medical emergency, notification is made by email or phone no later than the day of the exam. In the case of medical emergency, a written doctor's excuse may be required.
- Homework will be assigned at the end of each class and will be due one week from the day assigned. Late homework will be accepted up to one week past the due date. Greater than one week past due will not be accepted.
- Quizzes will be announced one class period ahead of the day of the quiz.

Course Schedule

Week	Dates	Topic(s)	Homework
1	Aug. 17, 19	Number systems and conversions, arithmetic operations.	Chap 1
2	Aug. 24, 26	Boolean algebra, combinational logic	Chap 2
3	Aug. 31, 2	Algebraic simplification of Boolean expressions	Chap 3,4
4	Sep. 7, 9	No class Sep. 7, Karnaugh maps and minimization	Chap 5
5	Sep. 14, 16	Exam 1 (Sep. 16) , Karnaugh maps	Chap 5
6	Sep. 21, 23	Quine-McKluskey method, multi-level gate circuits.	Chap 6,7
7	Sep. 28, 30	Combinational circuit design	Chap 8
8	Oct. 5, 7	Multiplexers and de-multiplexers, decoders and encoders	Chap 9
9	Oct. 12, 14	Exam 2 (Oct. 14) , Programmable logic devices (PLD, FPGA)	Chap 9
10	Oct. 19, 21	Latches and flip-flops.	Chap 11
11	Oct. 26, 28	Registers and counters.	Chap 12
12	Nov. 2, 4	Sequential circuit analysis.	Chap 13
13	Nov. 9, 11	Exam 3 (Nov. 11) , Sequential circuit analysis.	Chap 13
14	Nov. 16, 18	Sequential circuit design.	Chap 14
15	Nov. 23, 25	Fall break, no classes	
16	Nov. 30, 2	State reduction and assignment, optimization techniques	Chap 15
17	Dec. 7, 9	Final Exam (TBD)	

Students called for military duty

- “If you are a student in the military with the potential of being called to military service and /or training during the course of the semester, you are encouraged to contact Paul Rakowski in the Dean’s office.